CLAIMS:

1. A semiconductor storage device having a memory cell array (21), which employs a memory element constructed of a gate electrode (1104) formed on a semiconductor layer (1102) via a gate insulation film (1103), a channel region (1121) arranged under the gate electrode (1104), diffusion regions (1107a, 1107b) that are arranged on both sides of the channel region (1121) and have a conductive type opposite to that of the channel region (1121), and memory function bodies (1105a, 1105b) that are formed on both sides of the gate electrode (1104) and have a function to retain electric charges, as a memory cell,

the semiconductor storage device comprising:

a first switch (SW1) that has an input terminal to which an input voltage supplied from outside to the memory cell array is applied and has an output terminal connected to an input terminal of the memory cell array;

a second switch (SW2) that has an input terminal to which the input voltage is applied;

a charge pump (23) that has a pump input terminal connected to an output terminal of the second switch (SW2);

a third switch (SW3) that has an input terminal connected to a pump output terminal of the charge pump (23) and has an output terminal connected to the input terminal of the memory cell array (21);

an input voltage determining circuit (24) that determines whether or not the input voltage is not higher than a prescribed voltage; and

a control circuit (25) that turns on the first switch (SW1) and turns off the second and third switches (SW2, SW3) when the input voltage determining circuit (24) determines that the input voltage exceeds the prescribed voltage and turns off the first switch (SW1) and turns on the second and third switches (SW2, SW3) when the input voltage determining circuit determines that the input voltage is not higher than the prescribed voltage.

2. The semiconductor storage device as claimed in claim 1, wherein

each of the first, second and third switches (SW1, SW2, SW3) comprises:

a first P-channel field-effect transistor (31) that has a source forming an input terminal (Vin);

a second P-channel field-effect transistor (32) that has a drain connected to a drain of the first P-channel field-effect transistor (31) and a source forming an output terminal (Vout);

a first voltage level shifter (33) that selectively connects a gate of the first P-channel field-effect transistor (31) to either its source or ground

according to a control signal from the control circuit (25); and

a second voltage level shifter (34) that selectively connects a gate of the second P-channel field-effect transistor (32) to either its source or ground according to a control signal from the control circuit (25).

3. The semiconductor storage device as claimed in claim 1, wherein

the prescribed voltage is a voltage within a range of +3 V to +12 V.

4. The semiconductor storage device as claimed in any one of claims 1 through 3, comprising:

a voltage polarity inverter circuit (26) that has an input terminal connected to the output terminal of the first switch (SW1) and inverts polarity of the voltage inputted to the input terminal to output the resulting voltage to the memory cell array (21).

5. A semiconductor storage device having a memory cell array (21), which employs a memory element constructed of a gate electrode (1104) formed on a semiconductor layer (1102) via a gate insulation film (1103), a channel region (1121) arranged under the gate electrode (1104), diffusion regions (1107a, 1107b) that are arranged on both sides of the channel region (1121) and have a conductive type

opposite to that of the channel region (1121), and memory function bodies (1105a, 1105b) that are formed on both sides of the gate electrode (1104) and have a function to retain electric charges, as a memory cell,

a first switch (SW1) that has an input terminal to which the input voltage of negative polarity supplied from outside to the memory cell array (21) is applied and has an output terminal connected to the input terminal of the memory cell array (25);

a second switch (SW2) that has an input terminal to which the input voltage of the negative polarity is applied;

a charge pump (23) that has a pump input terminal connected to an output terminal of the second switch (SW2);

a third switch (SW3) that has an input terminal connected to a pump output terminal of the charge pump (23) and has an output terminal connected to the input terminal of the memory cell array (21);

an input voltage determining circuit (24) that determines whether or not the input voltage is not lower than a prescribed voltage; and

a control circuit (25) that turns on the first switch (SW1) and turns off the second and third switches (SW2, SW3) when the input voltage determining circuit (24) determines that the input voltage is lower than the

prescribed voltage and turns off the first switch (SW1) and turns on the second and third switches (SW2, SW3) when the input voltage determining circuit (24) determines that the input voltage is not lower than the prescribed voltage.

6. The semiconductor storage device as claimed in claim 5, wherein

each of the first, second and third switches (SW1, SW2, SW3) comprises:

a first N-channel field-effect transistor (31) that has a source forming an input terminal (Vin);

a second N-channel field-effect transistor (32) that has a drain connected to a drain of the first N-channel field-effect transistor (31) and a source forming an output terminal (Vout);

a first voltage level shifter (33) that selectively connects a gate of the first N-channel field-effect transistor (31) to either its source or ground according to a control signal from the control circuit (25); and

a second voltage level shifter (34) that selectively connects a gate of the second N-channel field-effect transistor (32) to either its source or ground according to a control signal from the control circuit (25).

7. The semiconductor storage device as claimed in claim 5, wherein

the prescribed voltage is a voltage within a range of -3 V to -12 V.

8. A semiconductor storage device having a memory cell array (21), which employs a memory element constructed of a gate electrode (1104) formed on a semiconductor layer (1102) via a gate insulation film (1103), a channel region (1121) arranged under the gate electrode (1104), diffusion regions (1107a, 1107b) that are arranged on both sides of the channel region (1121) and have a conductive type opposite to that of the channel region (1121), and memory function bodies (1105a, 1105b) that are formed on both sides of the gate electrode (1104) and have a function to retain electric charges, as a memory cell,

a first switch (SW1) that has an input terminal to which an input voltage of positive polarity supplied from outside to the memory cell array (21) is applied and has an output terminal connected to the input terminal of the memory cell array;

a second switch (SW2) that has an input terminal to which the input voltage of the positive polarity is applied;

a first charge pump (23) that has a pump input terminal connected to the output terminal of the second switch;

a third switch (SW3) that has an input terminal connected to an output terminal of the first charge pump (23) and has an output terminal connected to the input terminal of the memory cell array (21);

a first input voltage determining circuit (24) that determines whether or not the input voltage of the positive polarity is not higher than a first prescribed voltage;

a first control circuit (25) that turns on the first switch (SW1) and turns off the second and third switches (SW2, SW3) when the first input voltage determining circuit (24) determines that the input voltage of the positive polarity exceeds the first prescribed voltage and turns off the first switch (SW1) and turns on the second and third switches (SW2, SW3) when the first input voltage determining circuit determines that the input voltage of the positive polarity is not higher than the first prescribed voltage;

a fourth switch that has an input terminal to which an input voltage of negative polarity supplied from outside to the memory cell array is applied and has an

output terminal connected to the input terminal of the memory cell array;

a fifth switch that has an input terminal to which the input voltage of the negative polarity is applied;

a second charge pump that has a pump input terminal connected to an output terminal of the fifth switch;

a sixth switch that has an input terminal connected to an output terminal of the second charge pump and has an output terminal connected to the input terminal of the memory cell array;

a second input voltage determining circuit that determines whether or not the input voltage of the negative polarity is not lower than a second prescribed voltage; and

a second control circuit that turns on the fourth switch and turns off the fifth and sixth switches when the second input voltage determining circuit determines that the input voltage of the negative polarity is lower than the second prescribed voltage and turns off the fourth switch and turns on the fifth and sixth switches when the second input voltage determining circuit determines that the input voltage of the negative polarity is not lower than the second prescribed voltage.

9. The semiconductor storage device as claimed in claim 8, wherein

each of the first, second and third switches (SW1, SW2, SW3) comprises:

a first P-channel field-effect transistor (31) that has a source forming an input terminal (Vin);

a second P-channel field-effect transistor (32) that has a drain connected to a drain of the first P-channel field-effect transistor (31) and a source forming an output terminal (Vout);

a first voltage level shifter (33) that selectively connects a gate of the first P-channel field-effect transistor (31) to either its source or ground according to a control signal from the first control circuit (25); and

a second voltage level shifter (34) that selectively connects a gate of the second P-channel field-effect transistor (32) to either its source or ground according to a control signal from the first control circuit (25), wherein

each of the fourth, fifth and sixth switches comprises:

a first N-channel field-effect transistor that has a source forming an input terminal;

a second N-channel field-effect transistor that has a drain connected to a drain of the first N-channel field-effect transistor and a source forming an output terminal;

a third voltage level shifter that selectively connects a gate of the first N-channel field-effect transistor to either its source or ground according to a control signal from the second control circuit; and

a fourth voltage level shifter that selectively connects a gate of the second N-channel field-effect transistor to either its source or ground according to a control signal from the second control circuit.

10. The semiconductor storage device as claimed in claim 8, wherein

the prescribed first voltage is a voltage within a range of +3 V to +12 V, and

the prescribed second voltage is a voltage within a range of -3 V to -12 V.

11. A semiconductor storage device comprising:

a memory cell array (21);

a first switch (SW1) that has an input terminal to which an input voltage supplied from outside to the memory cell array is applied and has an output terminal connected to an input terminal of the memory cell array;

a second switch (SW2) that has an input terminal to which the input voltage is applied;

a charge pump (23) that has a pump input terminal connected to an output terminal of the second switch (SW2);

a third switch (SW3) that has an input terminal connected to a pump output terminal of the charge pump (23) and has an output terminal connected to the input terminal of the memory cell array (21);

an input voltage determining circuit (24) that determines whether or not the input voltage is not lower than a prescribed voltage; and

a control circuit (25) that turns on the first switch (SW1) and turns off the second and third switches (SW2, SW3) when the input voltage determining circuit (24) determines that the input voltage is lower than the prescribed voltage and turns off the first switch (SW1) and turns on the second and third switches (SW2, SW3) when the input voltage determining circuit determines that the input voltage is not lower than the prescribed voltage.

12. A semiconductor storage device comprising:

a memory cell array (21);

a first switch (SW1) that has an input terminal to which an input voltage of positive polarity supplied from outside to the memory cell array (21) is applied and

has an output terminal connected to the input terminal of the memory cell array;

a second switch (SW2) that has an input terminal to which the input voltage of the positive polarity is applied;

a first charge pump (23) that has a pump input terminal connected to the output terminal of the second switch;

a third switch (SW3) that has an input terminal connected to an output terminal of the first charge pump (23) and has an output terminal connected to the input terminal of the memory cell array (21);

a first input voltage determining circuit (24) that determines whether or not the input voltage of the positive polarity is not higher than a first prescribed voltage;

a first control circuit (25) that turns on the first switch (SW1) and turns off the second and third switches (SW2, SW3) when the first input voltage determining circuit (24) determines that the input voltage of the positive polarity exceeds the first prescribed voltage and turns off the first switch (SW1) and turns on the second and third switches (SW2, SW3) when the first input voltage determining circuit determines that the input

voltage of the positive polarity is not higher than the first prescribed voltage;

a fourth switch that has an input terminal to which an input voltage of negative polarity supplied from outside to the memory cell array is applied and has an output terminal connected to the input terminal of the memory cell array;

a fifth switch that has an input terminal to which the input voltage of the negative polarity is applied;

a second charge pump that has a pump input terminal connected to an output terminal of the fifth switch;

a sixth switch that has an input terminal connected to an output terminal of the second charge pump and has an output terminal connected to the input terminal of the memory cell array;

a second input voltage determining circuit that determines whether or not the input voltage of the negative polarity is not lower than a second prescribed voltage; and

a second control circuit that turns on the fourth switch and turns off the fifth and sixth switches when the second input voltage determining circuit determines that the input voltage of the negative polarity is lower than the second prescribed voltage and turns off the fourth

switch and turns on the fifth and sixth switches when the second input voltage determining circuit determines that the input voltage of the negative polarity is not lower than the second prescribed voltage.

13. The semiconductor storage device as claimed in claim 1, wherein at least part of the memory function bodies owned by the memory element overlaps with part of the diffusion region.

14. The semiconductor storage device as claimed in claim 1, comprising: an insulation film (1241), which separates a film (1242), that has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, from the channel region or the semiconductor layer (1211), the insulation film (1241) having a film thickness (T1) thinner than a film thickness (T2) of the gate insulation film (1214) and being not smaller than 0.8 nm.

15. Portable electronic equipment having the semiconductor storage device claimed in claim 1.